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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/635,373	08/06/2003	Richard W. Adkisson	200209002-1	1277

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EXAMINER	
BRITT, CYNTHIA H	
ART UNIT	**PAPER NUMBER**
2117	

SHORTENED STATUTORY PERIOD OF RESPONSE	MAIL DATE	DELIVERY MODE
3 MONTHS	04/06/2007	PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

If NO period for reply is specified above, the maximum statutory period will apply and will expire 6 MONTHS from the mailing date of this communication.

Office Action Summary	Application No.	Applicant(s)	
	10/635,373	ADKISSON ET AL.	
	Examiner	Art Unit	
	Cynthia Britt	2138	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☐ Responsive to communication(s) filed on _____.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-25* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-25* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *06 August 2003* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date *8/6/03, and 5/19/05*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Information Disclosure Statement

The information disclosure statements (IDS) submitted on 8/6/03, and 5/19/05 have been considered by the examiner. Forms 1449 have been signed and returned with this office action.

Drawings

The drawings received on 8/6/03 are acceptable.

Double Patenting

The nonstatutory double patenting rejection is based on a judicially created doctrine grounded in public policy (a policy reflected in the statute) so as to prevent the unjustified or improper timewise extension of the "right to exclude" granted by a patent and to prevent possible harassment by multiple assignees. A nonstatutory obviousness-type double patenting rejection is appropriate where the conflicting claims are not identical, but at least one examined application claim is not patentably distinct from the reference claim(s) because the examined application claim is either anticipated by, or would have been obvious over, the reference claim(s). See, e.g., *In re Berg*, 140 F.3d 1428, 46 USPQ2d 1226 (Fed. Cir. 1998); *In re Goodman*, 11 F.3d 1046, 29 USPQ2d 2010 (Fed. Cir. 1993); *In re Longi*, 759 F.2d 887, 225 USPQ 645 (Fed. Cir. 1985); *In re Van Ornum*, 686 F.2d 937, 214 USPQ 761 (CCPA 1982); *In re Vogel*, 422 F.2d 438, 164 USPQ 619 (CCPA 1970); and *In re Thorington*, 418 F.2d 528, 163 USPQ 644 (CCPA 1969).

A timely filed terminal disclaimer in compliance with 37 CFR 1.321(c) or 1.321(d) may be used to overcome an actual or provisional rejection based on a nonstatutory double patenting ground provided the conflicting application or patent either is shown to be commonly owned with this application, or claims an invention made as a result of activities undertaken within the scope of a joint research agreement.

Effective January 1, 1994, a registered attorney or agent of record may sign a terminal disclaimer. A terminal disclaimer signed by the assignee must fully comply with 37 CFR 3.73(b).

Claims 1-25 are provisionally rejected on the ground of nonstatutory obviousness-type double patenting as being unpatentable over claims 1-12 of

copending Application No. 10/635083. Although the conflicting claims are not identical, they are not patentably distinct from each other because:

The present independent claim 1 recites

1. A match circuit for implementation in a general purpose performance counter ("GPPC") connected to a bus carrying debug data, the match circuit comprising logic for activating a match signal when a selected N-bit portion of the debug data matches an N-bit threshold for all bits selected by an N-bit match mask ("mmask")

Claim 1 from the copending application recites

1. A general purpose performance counter ("GPPC") connected to a bus carrying debug data, the GPPC comprising: an AND/OR circuit connected to receive the debug data; a counter circuit connected to receive from the AND/OR circuit an increment signal that, when activated, causes the counter circuit to increment a current count value; and a compare circuit for activating a match/threshold signal to the AND/OR circuit responsive to a selected block of the debug data having a designated relationship to a compare value, wherein the AND/OR circuit activates the increment signal responsive to one or more selected bits of an events signal being set

A person having ordinary skill in the art at the time this invention was made would have known that a logic combination of AND/OR circuitry has been commonly used in the art as a comparison circuit to determine whether signals match and would therefore have been obvious to use such logic as a 'match' circuit.

Claim 2 of the present application recites;

2. The match circuit of claim 1 wherein N is equal to sixteen.

Claim 12 of the copending application recites;

12. The GPPC of claim 1 wherein the selected block comprises 16 bits and the debug data comprises eight 10-bit-block-aligned blocks.

Claims 3 and 4 of the present application recite;

3. The match circuit of claim 1 wherein the N-bit threshold is provided from a control status register ("CSR").

4. The match circuit of claim 1 wherein the N-bit mmask is provided from a control status register ("CSR").

This would be an obvious variation of sending a control signal as is typically used in the prior arts of record. The naming of a register through which a signal is sent does not cause it to become novel to send a signal through a register.

Claim 5 of the present application recites;

5. The match circuit of claim 1 wherein the debug data comprises 80 bits.

Claim 11 of the copending application recites

11. The GPPC of claim 1 wherein the debug data comprises 80 bits.

Claims 6 and 7 of the present application recites;

6. The match circuit of claim 5 wherein the debug data comprises eight 16-bit portions aligned on 10-bit blocks.

7. The match circuit of claim 6 wherein the selected portion comprises one of the eight 16-bit portions.

Claim 12 of the copending application recites

12. The GPPC of claim 1 wherein the selected block comprises 16 bits and the debug data comprises eight 10-bit-block-aligned blocks.

Claim 8 of the present application recites;

8. The match circuit of claim 1 wherein the logic for activating a match signal comprises logic for comparing a binary bit of the selected debug data portion with a corresponding bit of the threshold and outputting a binary bit indicative of whether the compared bits match.

Claim 2 of the copending application recites;

2. The GPPC of claim 1 wherein the compare circuit comprises a match circuit for activating the match/threshold signal to the AND/OR circuit when the compare circuit is in match mode and the selected debug data block is equal to the compare value.

As stated in the comments regarding claim 1, a person having ordinary skill in the art at the time this invention was made would have known that a logic combination of AND/OR circuitry has been commonly used in the art as a comparison circuit to determine whether signals match and would therefore have been obvious to use such logic as a 'match' circuit.

The remaining claims 9-25 are also obvious variations of the recited claims above for the same reasons.

This is a provisional obviousness-type double patenting rejection because the conflicting claims have not in fact been patented.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Cynthia Britt whose telephone number is 571-272-3815. The examiner can normally be reached on Monday - Thursday.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Albert Decady can be reached on 571-272-3819. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

Cynthia Britt
Primary Examiner
Art Unit 2138